TinyLogic UHS Unbuffered Inverter

NC7SZU04

Description

The NC7SZU04 is a single unbuffered inverter from **onsemi**'s Ultra−High Speed series of TinyLogic. The special purpose unbuffered circuit design is primarily intended for crystal oscillator or analog applications. The device is fabricated with advanced CMOS technology to achieve ultra−high speed with high output drive while maintaining low static power dissipation over a broad V_{CC} operating range. The device is specified to operate over the 1.65 V to 5.5 V V_{CC} range.

Features

- Unbuffered for Crystal Oscillator and Analog Applications
- Balanced Output Drive: ±32 mA at 4.5 V V_{CC}
- Balanced Output Drive: ±16 mA at 4.5 V V_{CC} (NC7SZU04P5X−L22057)
- Broad V_{CC} Operating Range: 1.65 V to 5.5 V
- Matches Performance of LCX Operated at 3.3 V V_{CC}
- Low Quiescent Power: I_{CC} < 2 μA, V_{CC} = 5.5 V, T_A = 25°C
- Ultra−Small MicroPak™ Packages
- Space−Saving SOT−23−5 and SC−88A Packages
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

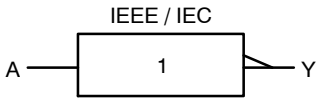
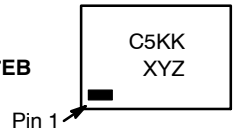


Figure 1. Logic Symbol

MARKING DIAGRAMS

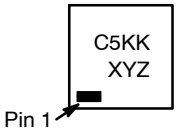


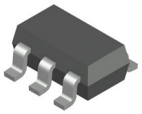
SIP6
CASE 127EB



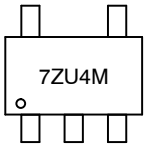


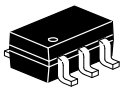
UDFN6
CASE 517DP



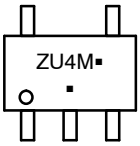


SOT−23−5
CASE 527AH





SC−88A
CASE 419A−02



C5, 7ZU4, ZU4 = Specific Device Code
KK = 2−Digit Lot Run Traceability Code
XY = 2−Digit Date Code Format
Z = Assembly Plant Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 7 of this data sheet.

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Pin Configurations

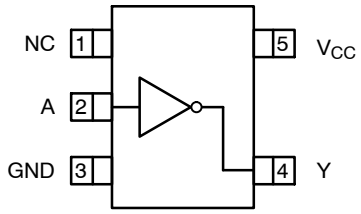


Figure 2. SC88A and SOT−23−5 (Top View)

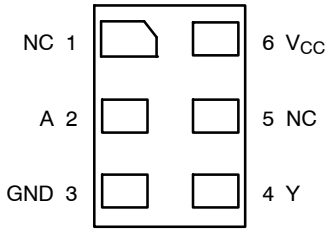


Figure 3. MicroPak (Top Through View)

PIN DEFINITIONS

Pin # SC−88A / SOT−23−5	Pin # MicroPak	Name	Description
1	1, 5	NC	No Connect
2	2	A	Input
3	3	GND	Ground
4	4	Y	Output
5	6	V_{CC}	Supply Voltage

FUNCTION TABLE

Inputs	Output
A	**Y**
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		−0.5	6.5	V
V_{IN}	DC Input Voltage		−0.5	6.5	V
V_{OUT}	DC Output Voltage		−0.5	V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	V_{IN} < 0 V	−	−50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < 0 V	−	−50	mA
		V_{OUT} > V_{CC}	−	+50	
I_{OUT}	DC Output Current		−	±50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current		−	±50	mA
T_{STG}	Storage Temperature Range		−65	+150	°C
T_J	Junction Temperature Under Bias		−	+150	°C
T_L	Junction Lead Temperature (Soldering, 10 Seconds)		−	+260	°C
P_D	Power Dissipation in Still Air	SOT−23−5	−	390	mW
		SC−88A	−	332	
		MicroPak−6	−	812	
		MicroPak2™−6	−	812	
ESD	Human Body Model, JEDEC: JESD22−A114		−	4000	V
	Charge Device Model, JEDEC: JESD22−C101		−	2000	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage Operating		1.65	5.5	V
	Supply Voltage Data Retention		1.50	5.5	
V_{IN}	Input Voltage		0	5.5	V
V_{OUT}	Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		−40	+85	°C
θ_{JA}	Thermal Resistance	SOT−23−5	−	320	°C/W
		SC−88A	−	377	
		MicroPak−6	−	154	
		MicroPak2−6	−	154	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Unused inputs must be held HIGH or LOW. They may not float.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = +25°C			T_A = −40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	HIGH Level Input Voltage		1.8 to 2.7	0.85 V_{CC}	–	–	0.85 V_{CC}	–	V
			3.0 to 5.5	0.80 V_{CC}	–	–	0.80 V_{CC}	–	
V_{IL}	LOW Level Input Voltage		1.8 to 2.7	–	–	0.15 V_{CC}	–	0.15 V_{CC}	V
			3.0 to 5.5	–	–	0.20 V_{CC}	–	0.20 V_{CC}	
V_{OH}	High−Level Output Voltage	V_{IN} = GND I_{OH} = −100 μA I_{OH} = −4 mA I_{OH} = −8 mA I_{OH} = −12 mA I_{OH} = −16 mA I_{OH} = −24 mA I_{OH} = −32 mA	 1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5	 V_{CC} − 0.1 1.29 1.9 2.2 2.4 2.3 3.8	 V_{CC} 1.4 2.1 2.4 2.7 2.5 4.0	 – – – – – – –	 V_{CC} − 0.1 1.29 1.9 2.2 2.4 2.3 3.8	 – – – – – – –	V
V_{OL}	Low−Level Output Voltage	V_{IN} = V_{CC} I_{OL} = 100 μA I_{OL} = 4 mA I_{OL} = 8 mA I_{OL} = 12 mA I_{OL} = 16 mA I_{OL} = 24 mA I_{OL} = 32 mA	 1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5	 – – – – – – – –	 – 0.08 0.2 0.22 0.28 0.38 0.42	 0.1 0.24 0.3 0.4 0.4 0.55 0.55	 – – – – – – –	 0.1 0.24 0.3 0.4 0.4 0.55 0.55	V
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V, GND	1.65 to 5.5	–	–	±1	–	±10	μA
I_{CC}	Quiescent Supply Current	V_{IN} = 5.5 V, GND	1.65 to 5.5	–	–	2	–	20	μA
I_{CCPEAK}	Peak Supply Current in Analog Operation	V_{OUT} = Open, V_{IN} = Adjust for Peak I_{CC} Current	1.8	–	2	–	–	–	mA
			2.5	–	4	–	–	–	
			3.3	–	10	–	–	–	
			5.0	–	30	–	–	–	

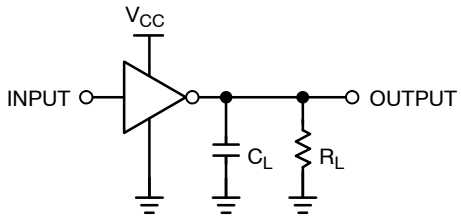
DC ELECTRICAL CHARACTERISTICS (NC7SZU04P5X−L22057, NC7SZU04L6X−L22175, NC7SZU04FHX−L22175)

Symbol	Parameter	V_{CC} (V)	Conditions		T_A = +25°C			T_A = −40 to +85°C		Unit
					Min	Typ	Max	Min	Max	
V_{IH}	HIGH Level Input Voltage	1.8 to 2.7			0.85 V_{CC}	–	–	0.85 V_{CC}	–	V
		3.0 to 5.5			0.80 V_{CC}	–	–	0.80 V_{CC}	–	
V_{IL}	LOW Level Input Voltage	1.8 to 2.7			–	–	0.15 V_{CC}	–	0.15 V_{CC}	V
		3.0 to 5.5			–	–	0.20 V_{CC}	–	0.20 V_{CC}	
V_{OH}	HIGH Level Output Voltage	1.65	V_{IN} = V_{IL}, I_{OH} = −100 μA		1.55	1.65	–	1.55	–	V
		1.80			1.60	1.80	–	1.60	–	
		2.30			2.10	2.30	–	2.10	–	
		3.00			2.70	3.00	–	2.70	–	
		4.50			4.00	4.40	–	4.00	–	
		1.65	V_{IN} = GND	I_{OH} = −4 mA	1.29	1.52	–	1.29	–	
		2.30		I_{OH} = −4 mA	1.90	2.14	–	1.90	–	
		3.00		I_{OH} = −8 mA	2.40	2.75	–	2.40	–	
		3.00		I_{OH} = −12 mA	2.30	2.61	–	2.30	–	
		4.50		I_{OH} = −16 mA	3.80	4.13	–	3.80	–	
V_{OL}	LOW Level Output Voltage	1.65	V_{IN} = V_{IH}, I_{OL} = 100 μA		–	0.00	0.10	–	0.10	V
		1.80			–	0.00	0.20	–	0.20	
		2.30			–	0.00	0.20	–	0.20	
		3.00			–	0.00	0.30	–	0.30	
		4.50			–	0.00	0.50	–	0.50	
		1.65	V_{IN} = V_{CC}	I_{OL} = 4 mA	–	0.80	0.24	–	0.24	
		2.30		I_{OL} = 4 mA	–	0.10	0.30	–	0.30	
		3.00		I_{OL} = 8 mA	–	0.17	0.40	–	0.40	
		3.00		I_{OL} = 12 mA	–	0.25	0.55	–	0.55	
		4.50		I_{OL} = 16 mA	–	0.226	0.55	–	0.55	
I_{IN}	Input Leakage Current	1.65 to 5.5	V_{IN} = 5.5 V, GND		–	–	±1	–	±10	μA
I_{CC}	Quiescent Supply Current	1.65 to 5.50	V_{IN} = 5.5 V, GND		–	–	2	–	20	μA
I_{CCPEAK}	Peak Supply Current in Analog Operation	1.8	V_{OUT} = Open, V_{IN} = Adjust for Peak I_{CC} Current		–	2	–	–	–	mA
		2.5			–	4	–	–	–	
		3.3			–	10	–	–	–	
		5.0			–	30	–	–	–	

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C			T_A = −40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay (Figure 4, 5)	1.65	C_L = 15 pF, R_L = 1 MΩ	–	–	11.7	–	12.1	ns
		1.80		–	–	8.5	–	9.0	
		2.50 ±0.20		–	–	6.2	–	6.5	
		3.30 ±0.30		–	–	4.5	–	4.8	
		5.00 ±0.50		–	–	3.9	–	4.1	
		3.30 ±0.30	C_L = 50 pF, R_L = 500 Ω	–	–	6.0	–	6.5	
		5.00 ±0.50		–	–	5.0	–	5.5	
C_{IN}	Input Capacitance	0.00		–	4.5	–	–	–	pF
C_{PD}	Power Dissipation Capacitance (Note 2) (Figure 6)	3.30		–	6.3	–	–	–	pF
		5.00		–	9.5	–	–	–	

2. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = (C_{PD})\ (V_{CC})\ (f_{IN}) + (I_{CC}static)$.



NOTE:
3. C_L includes load and stray capacitance.
4. Input PRR = 1.0 MHz; t_W = 500 ns

Figure 4. AC Test Circuit

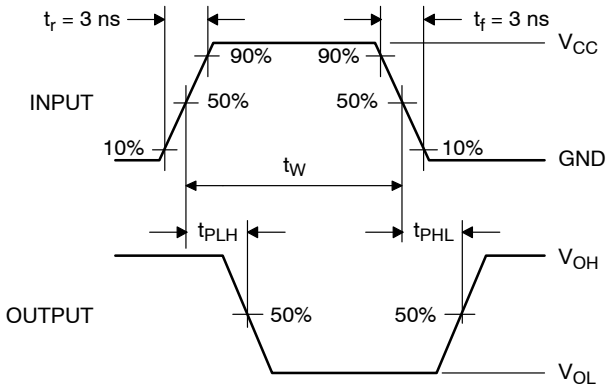
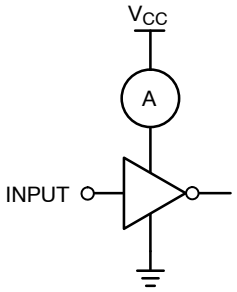


Figure 5. AC Waveforms



NOTE:
5. When operating the NC7SZU04's unbuffered output stage in its linear range, as in oscillator applications, care must be taken to observe maximum power rating for the device and package. The high drive nature of the design of the output stage results in substantial simultaneous conduction currents when the stage is in the linear region. *See the I_{CCPEAK} specification in the DC Electrical Characteristics table.*
6. Input = AC Waveform; $t_r = t_f$ = 1.8 ns; PRR = Variable; Duty Cycle = 50%.

Figure 6. I_{CCD} Test Circuit

ORDERING INFORMATION

Part Number	Top Mark	Packages	Shipping†
NC7SZU04M5X	7ZU4	SOT−23−5	3000 / Tape & Reel
NC7SZU04M5X−L22090	7ZU4	SOT−23−5	3000 / Tape & Reel
NC7SZU04P5X	ZU4	SC−88A	3000 / Tape & Reel
NC7SZU04P5X−L22057	ZU4	SC−88A	3000 / Tape & Reel
NC7SZU04L6X	C5	SIP6, MicroPak	5000 / Tape & Reel
NC7SZU04L6X−L22175	C5	SIP6, MicroPak	5000 / Tape & Reel
NC7SZU04FHX	C5	UDFN6, MicroPak2	5000 / Tape & Reel
NC7SZU04FHX−L22175	C5	UDFN6, MicroPak2	5000 / Tape & Reel

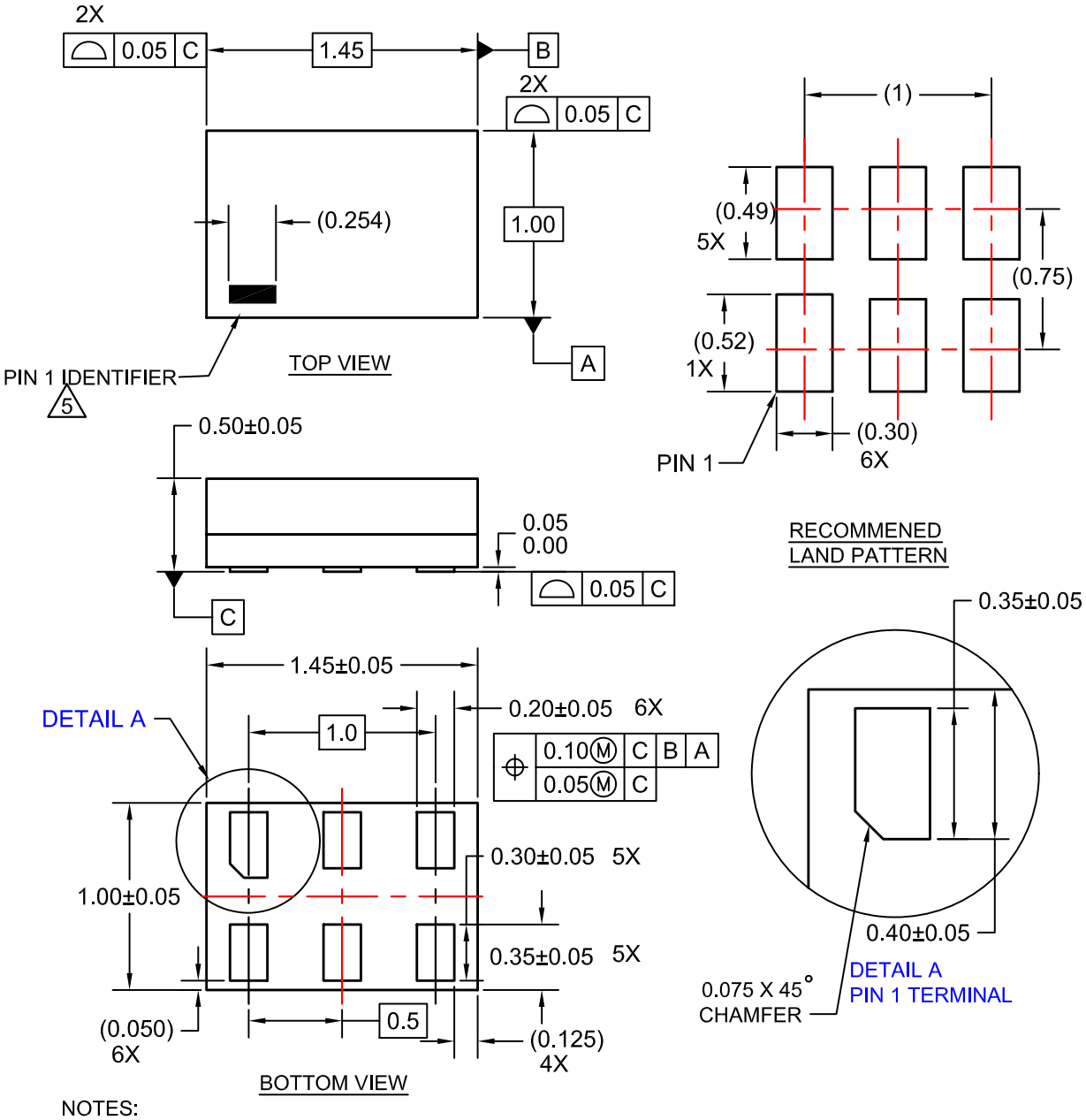
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SIP6 1.45X1.0
CASE 127EB
ISSUE O

DATE 31 AUG 2016



NOTES:

1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-2009
4. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

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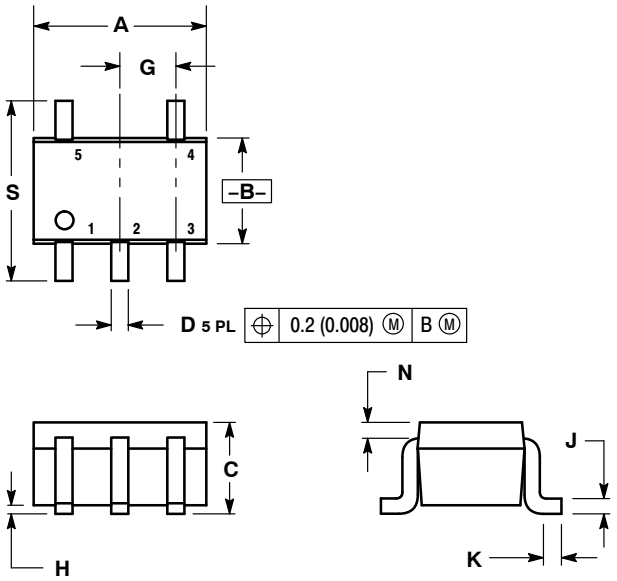
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE L

SCALE 2:1

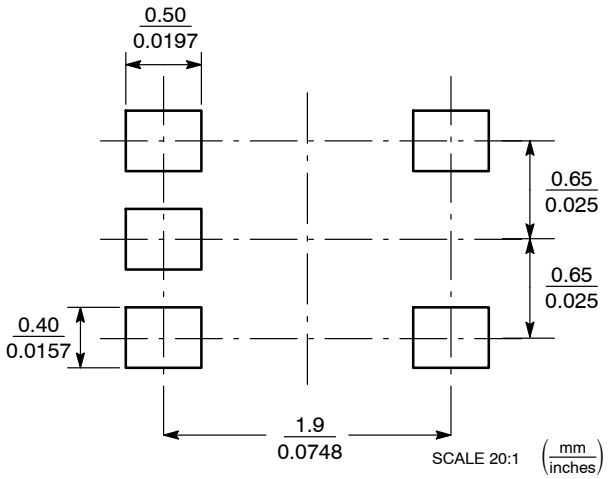
DATE 17 JAN 2013



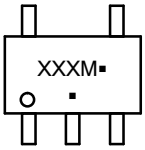
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1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

SOLDER FOOTPRINT



GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

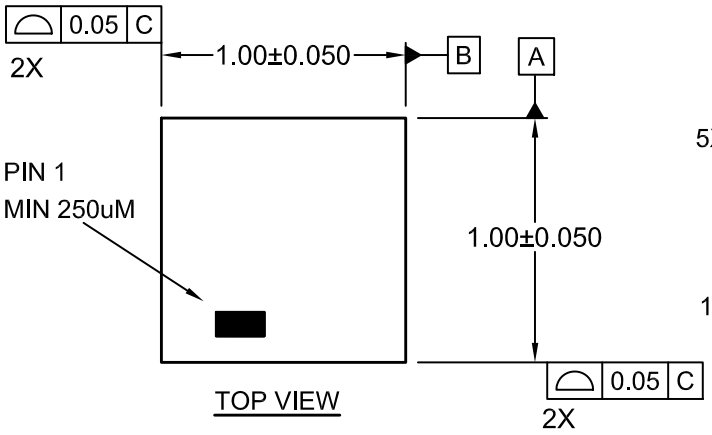
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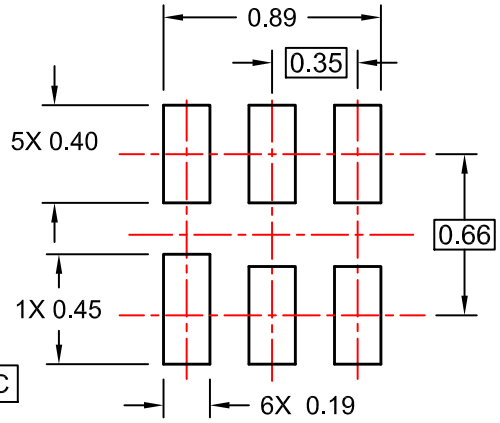
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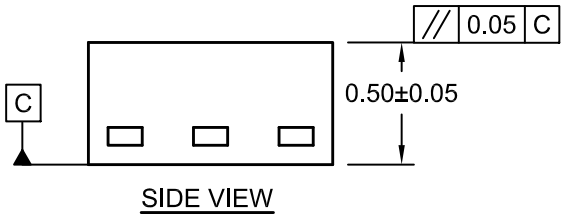
UDFN6 1.0X1.0, 0.35P
CASE 517DP
ISSUE O

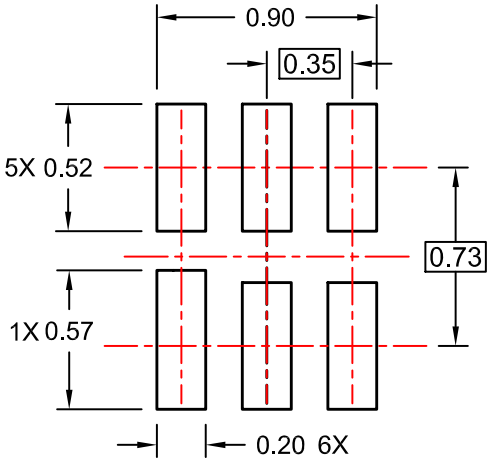
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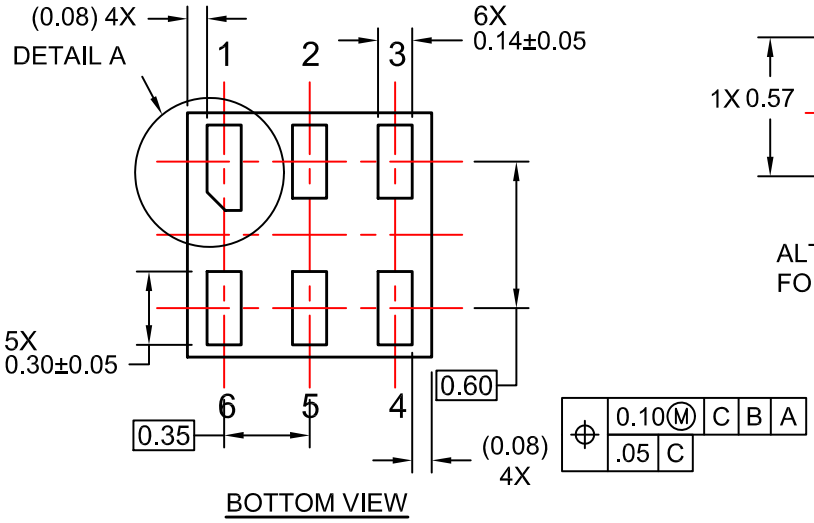


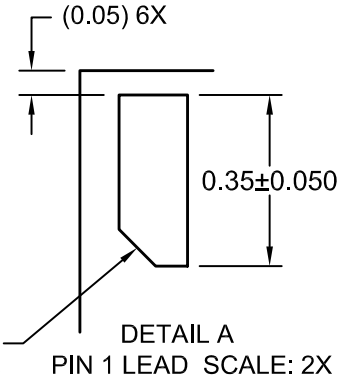
RECOMMENDED LAND PATTERN
FOR SPACE CONSTRAINED PCB





ALTERNATIVE LAND PATTERN
FOR UNIVERSAL APPLICATION





NOTES:

A. COMPLIES TO JEDEC MO-252 STANDARD
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009

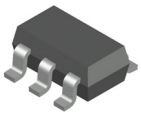
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DESCRIPTION:	**UDFN6 1.0X1.0, 0.35P**	**PAGE 1 OF 1**

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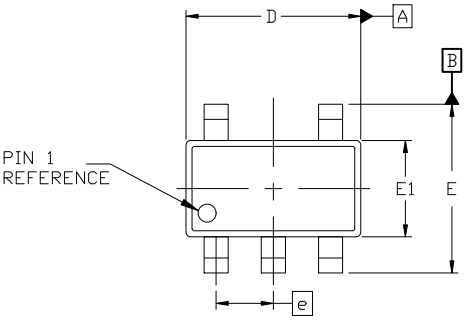
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

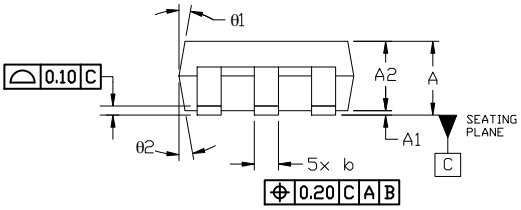


SOT−23, 5 Lead
CASE 527AH
ISSUE A

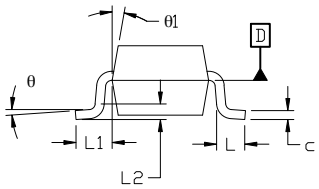
DATE 09 JUN 2021



TOP VIEW



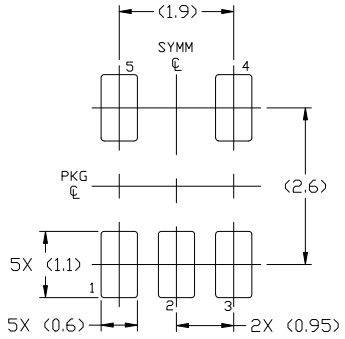
SIDE VIEW



END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 19894
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM D.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07mm.

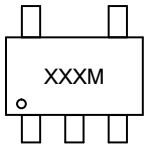
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.90	—	1.45
A1	0.00	—	0.15
A2	0.90	1.15	1.30
b	0.30	—	0.50
c	0.08	—	0.22
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 BSC		
L	0.30	0.45	0.60
L1	0.60 REF		
L2	0.25 REF		
θ	0°	4°	8°
θ1	0°	10°	15°
θ2	0°	10°	15°



RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**SOT−23, 5 LEAD**	**PAGE 1 OF 1**

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